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U.S. **UTILITY** Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10010343	12/05/2001	257		2811	

**APPLICANTS: Yegnashankaran Visvamohan; Padmanabhan Gobi;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☒	RESCIND ☐

Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no	072219-0261615 (P05089)
Verified and Acknowledged Examiner's initials		

TITLE : Integrated circuit and method of forming the integrated circuit having a die with high Q inductors and capacitors attached to a die with a circuit as a flip chip

U.S. DEPT. OF COMM./PAT. & TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING	
Amount Due	Date Paid		Sheets Drwg. / Figs.Drwg.	Print Fig.
		Primary Examiner		
☐ TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner	

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